ANALOG DEVICES

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APPLICATION NOTE

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Circuit Applications of the AD7226 Quad CMOS DAC

by Mike Byrne

The AD7226 is a monolithic quad 8-bit CMOS DAC packaged in a 20-pin DIP. Each DAC output is buffered by a CMOS amplifier which is capable of developing +10V across a 2kΩ resistor. Data is loaded from a common 8-bit data bus into one of the on-chip latches provided for each individual DAC (see Figure 1).

The AD7226 has certain features which make the part a unique and extremely useful device. Firstly, housing four DACs plus interface logic and output buffer amplifiers in a 20-pin package allows for substantial savings in circuit board space requirements and complexity. Additionally, the converters are operated in the voltage-mode which allows single supply operation for the part, with a unique DAC switch pair arrangement allowing an extended reference range not previously available with voltage-mode converters. Since all four DACs are fabricated on the same chip, precise matching and tracking between them is inherent.

This application note discusses some uses of the AD7226 in dc or voltage setting type applications. Operation of some of these circuits relies on the inherent DAC-to-DAC matching provided by the AD7226. Other circuits benefit from the circuit board space saving offered by the AD7226 and from its ability to operate with a single power supply.

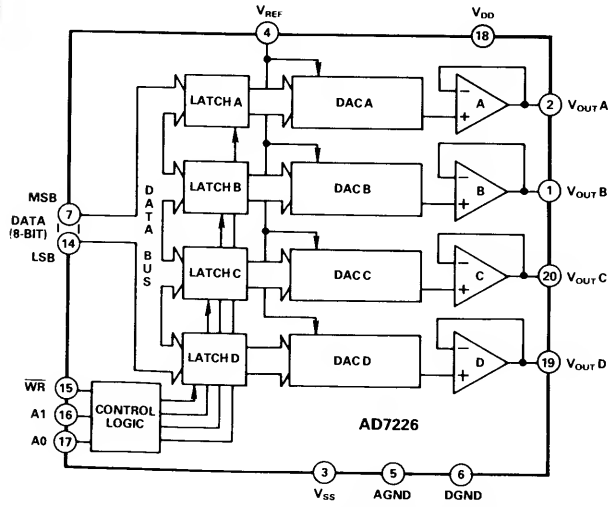

Figure 1. AD7226 Functional Diagram

This application note does not discuss the basic operation of the AD7226; consult the data sheet for this information.

AD7226 APPLICATIONS DISCUSSED IN THIS NOTE

1. Programmable Offset Adjust of Operational Amplifiers using one-channel of the quad DAC per op amp.
2. Set-Point Controller Circuit which allows fine adjust over a wide voltage range.
3. Self-Programmable Reference Voltage using one DAC of the AD7226.
4. Staircase Window Comparator Circuit for Measurement of Threshold Values for a TTL device.
5. V_{SS} Generation Circuits to allow dual supply operation of the AD7226 from a single power supply.
6. 5V Single Supply results showing excellent Differential Nonlinearity performance.

PROGRAMMABLE OFFSET ADJUST

The AD7226 can be used to provide programmable input offset voltage adjustment for operational amplifiers. The circuit configuration used to achieve this is shown in Figure 2. Each output of the AD7226 can be used to trim the input offset voltage of one operational amplifier. This means that programmable offset adjustment can be achieved on four operational amplifiers by the addition of just one 20-pin device and some extra resistors.

The circuit configuration uses the input offset voltage nulling pins provided on most operational amplifiers. Resistor R2, tied to +10V, provides a fixed bias current to one offset node. The output of the D/A converter is connected via R1 to provide a variable bias current to the other offset node. Therefore, changing the code on the D/A converter provides offset adjust for the operational amplifier. For symmetrical adjustment, the bias current through R2 should equal the current in the other offset node with the half-full scale code (i.e. 10000000) on the D/A converter.

Resistors R1 and R2 are chosen such that enough current variation over the DAC code range is given to provide the required range of offset adjustment for the op amp in question. Reducing the values of R1 and R2 increases the range of offset which can be trimmed, with a corresponding reduction in resolution.

The method of programmable offset adjustment can be used with most operational amplifiers which have offset

nulling pins provided. Table I shows some results achieved with four popular op amps. The table shows the typical range of offset values which can be trimmed using the given values of resistors R1 and R2. It also gives typical figures for final values of offset achieved after using the method outlined above.

The circuit configuration of Figure 2 ensures that, for increasing code on the D/A converter, the op amp offset goes more positive when using the first three op amps of Table I. For the TL091 and other op amps of the family (TL061, TL071, etc.) the trim terminals must be swopped (as indicated in Figure 3) to ensure that for increasing code the output offset will go in the positive direction.

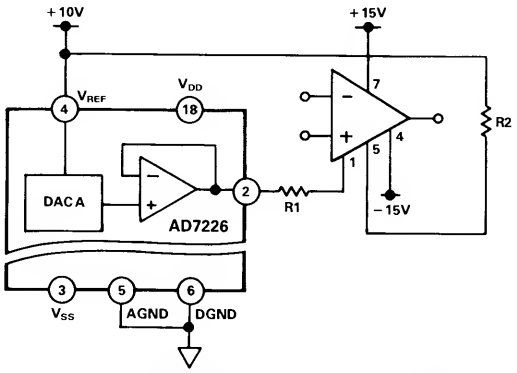

Figure 2. Offset Adjust Using AD7226

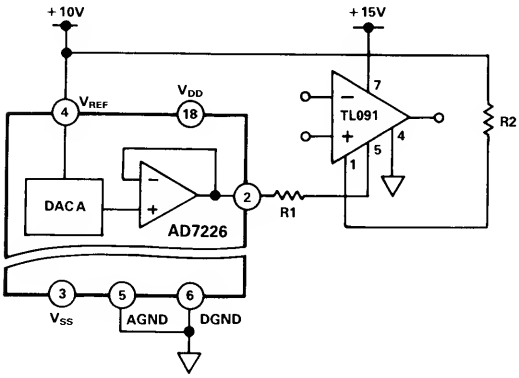

Figure 3. Offset Adjust for TL091

The trimming of op amp offsets in this manner increases the offset drift temperature coefficient of the op amp. For example, using the AD544 this increase will be 3μV/°C per millivolt of offset adjustment assuming 0ppm/°C temperature coefficient for the external resistors R1 and R2. However, the same drift would have been introduced had an external trimpot been used to trim the offset. The method outlined above has the advantage of being programmable and, therefore, any drift over temperature can be adjusted out during a periodic calibration cycle.

The programmable input offset voltage adjust can be used to deliberately introduce input offset voltage into the op amp. This could be useful in a system context where programmably introducing offset at a node in the system could give the desired value at the output of the system.

The first three op amps shown in Table I operate from dual supplies. The TL091 op amp is specified to operate at 5V single supply. The AD7226 can operate at 5V single supply and will remain monotonic to 8-bits under these conditions. This is basically all that is required for the configurations of Figure 2 and Figure 3 to function. The 5V single supply operation of the AD7226 is discussed later in this application note.

Op Amp	R2 (kΩ)	R1 (kΩ)	Range (mV)	Final Offset (μV)
AD741	1200	1000	±6.75	−14.5
AD544	620	500	±2.75	3.3
AD542	470	360	±2.4	4.6
TL091*	1000	500	+9.0	2.5

*Operating in Single Supply V_{SS} = 0V V_{DD} = +15V.
All other op amps dual supply ±15V.

Table I. Typical Op Amp Offset Results

Some operational amplifiers, especially duals and quads, do not have trim terminals available to the user. The AD7226 can still be used to provide offset adjustment by programmably varying the voltage at the required op amp input terminal. One such configuration is outlined in Figure 4. The noninverting input of the op amp is offset in a negative direction via R4 to −15V. In a similar fashion to the previous method, for symmetrical adjustment the current through R4 should equal the current through R3 with the half-full scale code on the D/A converter. Once again increasing the digital code will vary the offset in a positive direction. The resistor configuration will be seen as a low impedance by the noninverting input of the op amp to prevent noise injection. The circuit configuration does not affect the gain or transfer function of the op amp. Using the TL044 quad op amp, with the components values given in Figure 4, the typical range of offset which could be trimmed using the method outlined for Figure 3 was ±5.5mV. A typical figure for the final offset value achieved was 10μV. Similar techniques can be used for other op amp configurations.

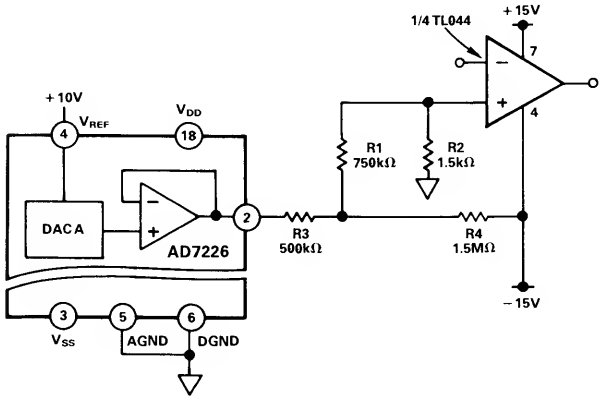

Figure 4. Alternative Offset Adjust

SET-POINT CONTROLLER

The set-point controller circuit of Figure 5 allows programmable fine and coarse adjust of the output voltage, V_{OUT}, over a 200V range. The circuit has a fine adjust resolution of 8mV which means that an output voltage can be set in the range −100V to +100V to within ±4mV.

The circuit uses DAC A as a programmable coarse adjust and DAC B as a programmable fine adjust of the output voltage. DAC A has an effective output voltage range of

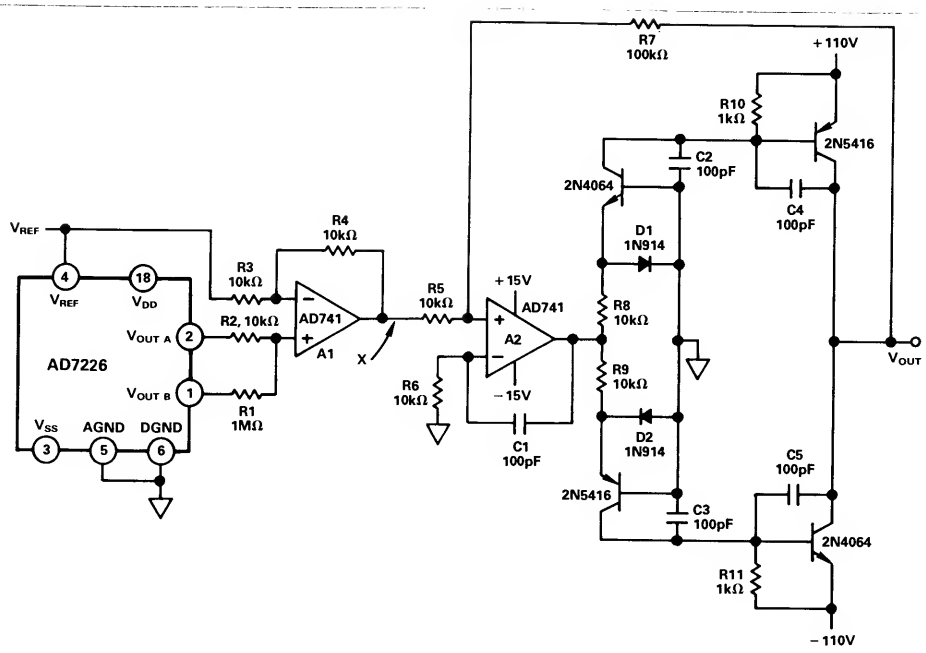

Figure 5. Set-Point Controller Circuit

−100V to +100V over the digital input code range giving an LSB size of 800mV for this coarse adjust DAC. DAC B has an effective output voltage range, at V_{OUT}, of 2V giving an LSB size of 8mV for this fine adjust DAC.

Amplifier A1 sums the output of both DACs and provides a bipolar output voltage, V_X, at point X. Amplifier A2, with the additional level shifting circuitry, provides a gain of 10 between V_X and V_{OUT}. In general, the output voltage V_{OUT} can be expressed as:

$$V_{OUT} = \frac{R_7}{R_5}\left\{ 2 \cdot V_{OUTA} \cdot \left(\frac{R_1}{R_1+R_2}\right) + 2 \cdot V_{OUTB} \cdot \left(\frac{R_2}{R_1+R_2}\right) - \left(V_{REF}\right)\right\}$$

For the component values given in the circuit of Figure 5 this can be simplified to give the expression for V_{OUT} as:

$$V_{OUT} = 10\left\{ V_{OUTA} \cdot \left(\frac{2000}{1010}\right) + V_{OUTB} \cdot \left(\frac{20}{1010}\right) - \left(V_{REF}\right)\right\}$$

The resolution of the fine adjust circuitry can be changed by varying R2. This is done without any significant effect on the overall output voltage range. Adjusting R7 will change the output voltage range, varying the resolution of both the fine adjust and coarse adjust DACs.

This circuit of Figure 5 is capable of developing ±100V across a 2.7kΩ load. It is useful in set-point controller applications or in a programmable power supply. The other two channels of the AD7226 can be used to perform normal D/A converter functions or configured as above to provide a second set-point controller.

SELF-PROGRAMMABLE REFERENCE

The circuit of Figure 6 shows how one D/A converter of the AD7226, in this case DAC A, may be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. The relationship of V_{REF} to V_{IN} is dependant upon digital code and upon the ratio of resistors R1 and R2. It can be expressed by the formula

$$V_{REF} = \frac{(1+G)}{1+G \cdot D_A} \cdot V_{IN}$$

where $G = {}^{R2}/_{R1}$

and D_A is a fractional representation of the digital word in latch A ($0 \leq D_A \leq 255/256$).

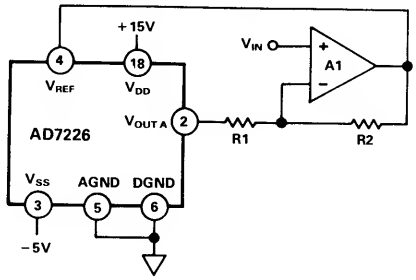

Figure 6. Self-Programmable Reference

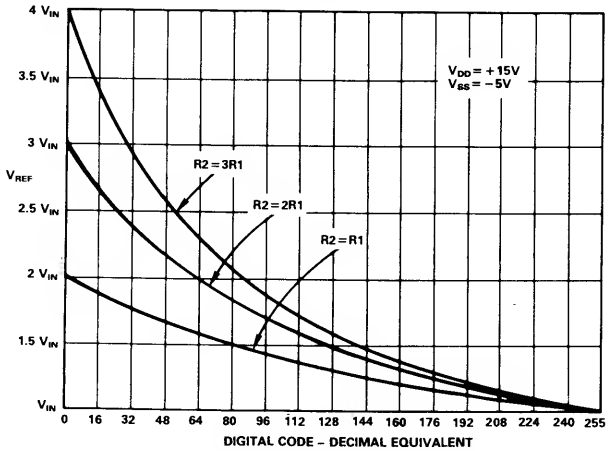

Figure 7. Variation of V_{REF} with Feedback Configuration

Figure 7 shows typical plots of V_{REF} versus digital code for three different values of R2. With V_{IN} = 2.5V and R2 = 3R1

the voltage at the output of A1 (i.e. reference voltage for the AD7226) will vary between +2.5V and +10V over the digital input code range. This gives an effective 10-bit dynamic range to the other three D/A converter outputs with the minimum LSB size being 10mV over a potential full scale output range of 0 to 10V.

The circuit of Figure 6 should only be used when the AD7226 is operated from dual supplies (i.e. $V_{SS} = -5V$). One reason for this is that the AD7226 is specified at +10V reference voltage only for single supply operation. More importantly, however, is the fact that the AD7226 has reduced current sink capability at output voltages near 0V when used in single supply (see AD7226 data sheet). This means that the circuit would not operate correctly at lower values of digital input code. For correct operation with dual supplies R1 must be greater than 6.8kΩ.

Different configurations of A1 and resistors can be devised to give other ranges of reference voltage. It must be noted that varying the voltage at the V_{REF} pin varies the reference voltage for all the converters. Whatever configuration devised must ensure that the voltage at the V_{REF} pin of the AD7226 must never go negative with respect to either AGND or DGND.

THRESHOLD TESTING

In test systems and other applications it is necessary to determine whether some unknown voltage lies within certain limits. In these cases the AD7226 can be used with external comparators or op amps to provide a programmable staircase window comparator. The voltage levels on the comparator and the window sizes are determined by the digital code in the latches of the D/A converters. Figure 8 shows one such application where the AD7226 can be used to measure the threshold levels of a TTL device under test.

V_{OUTA} and V_{OUTB} of the AD7226 in addition to the six external comparators, form a staircase window comparator. Each adjacent pair of comparators forms a window of programmable size. When a voltage lies within a window, the output from that window goes high . Window 1 is set with an upper limit of $V_{CC} = 5V$ and a lower limit of $V_{OUTA} = 2.4V$. Window 2 has an upper limit of 2.4V and a lower limit of 0.4V, while Window 3 has an upper limit of 0.4V and a lower limit of AGND = 0V. These levels can be programmably set and varied as required.

The staircase window comparator circuit is used in testing the output threshold levels of the device under test (DUT1). When D8 goes high, SW1 is set so that 400μA is sourced from the output of DUT1. The V_{OH} of DUT1 is applied to the staircase window comparator. For the part to pass its V_{OH} test, the output from Window 1 must go high. Any other window going high indicates that the device fails. When D8 goes low, SW1 is switched so that the output of DUT1 will sink 16mA and the V_{OL} of DUT1 is measured. Window 3 of the staircase window comparator must go high for the device to pass its V_{OL} test.

Window 2 is not really necessary in the application shown. However, it has been included to demonstrate the non-overlapping staircase comparator configuration. V_{OUTC} and V_{OUTD} of the AD7226, along with additional comparators, can be used to extend the staircase window comparator to give five programmable non-overlapping windows. The window structure for these five non-overlapping windows is shown in Figure 9 with the upper limit of the staircase now at V_{REF}. If overlapping windows are required, the configuration can easily be adapted as shown in Figure 10a. In this case all four outputs are used with the external comparators to provide three overlapping windows. The window structure for this overlapping window configuration is shown in Figure 10b.

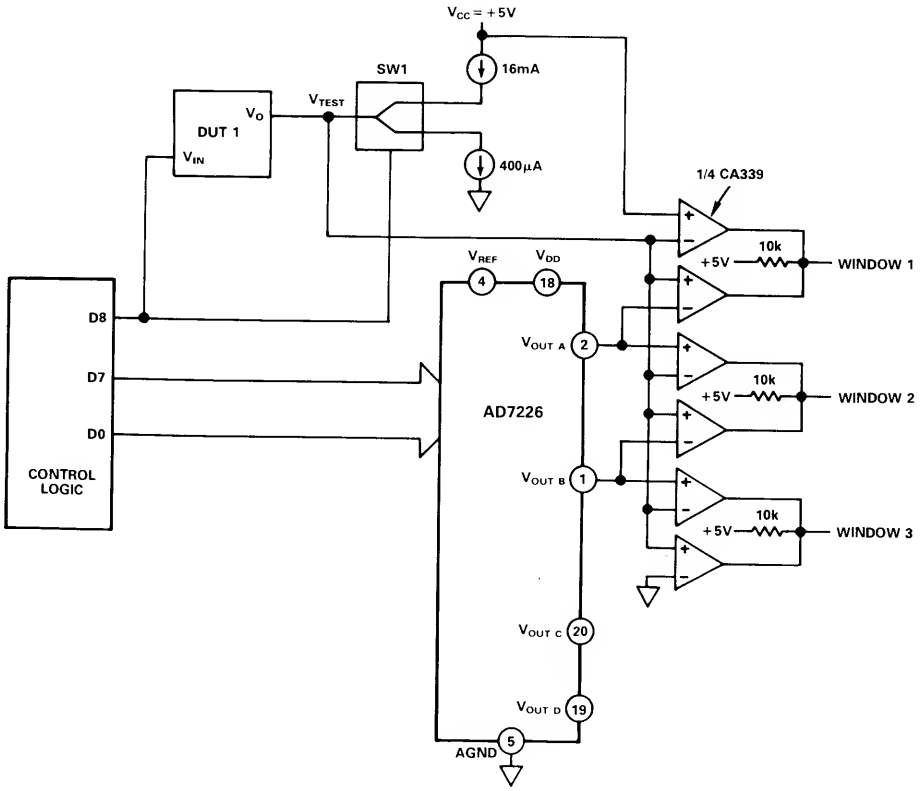

Figure 8. Threshold Testing

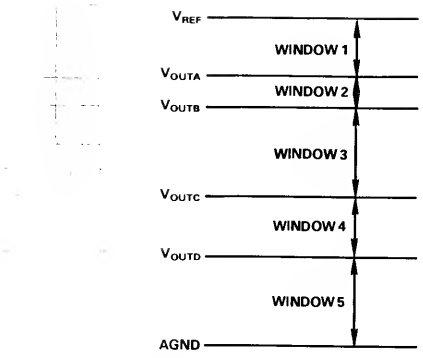

Figure 9. Window Structure

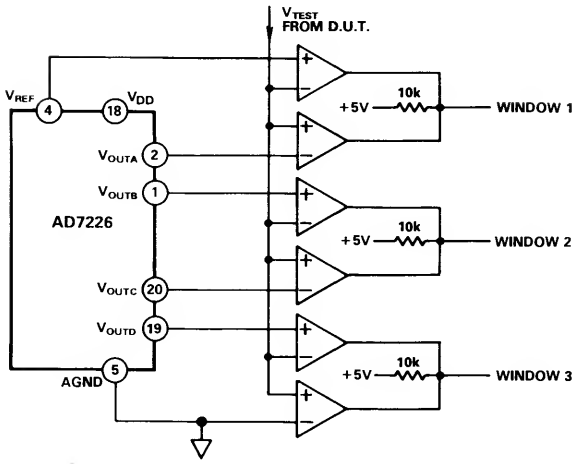

Figure 10a. Overlapping Windows

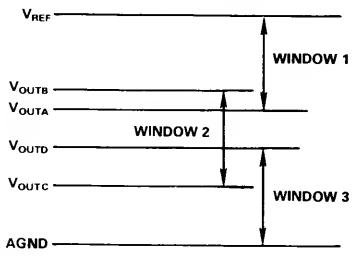

Figure 10b. Window Structure

V_{SS} GENERATION

Operating the AD7226 from dual supplies results in enhanced performance over single supply operation on a number of parameters. The negative V_{SS} gives additional headroom to the output amplifier which results in improved negative-going settling-time, improved zero code error performance and an extended input reference range. Some applications may require this enhanced performance but may only have a single power supply rail available. The following circuits show some methods of generating a negative V_{SS} from a single power supply rail for the AD7226.

Figure 11 shows one such method of generating a negative supply using one CD4049, operated from a V_{DD} of +15V. Two inverters of the hex inverter chip are used as an oscillator. The other four inverters are paralleled and used as buffers for higher output current. The square-wave output is level translated to a negative-going signal, then rectified and filtered. The circuit configuration shown will provide an output voltage of −5.1V for current loadings in the range of 0.5mA to 8mA. This will satisfy the AD7226 I_{SS} requirement over the commercial operating temperature range. Noise spikes which are generated on this V_{SS} line from the clock can be considerably reduced by decoupling the V_{DD} supply line to the CD4049.

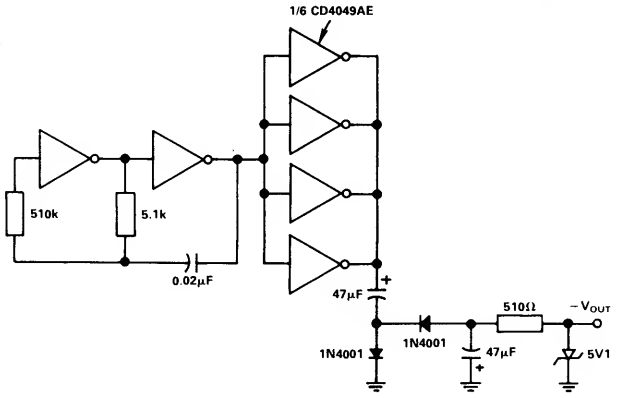

Figure 11. V_{SS} Generation Circuit

An alternative method of generating a negative supply from a positive rail is to use Analog Devices AD7560, a DC-DC voltage converter. This can provide a −5V supply from a +5V rail. The circuit configuration used to achieve this is outlined in Figure 12.

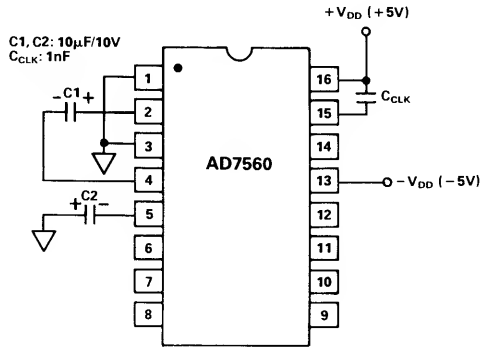

Figure 12. AD7560 Giving −5V

Some applications may require a +5V reference but may only have a single supply rail available. The AD7226 is specified at +5V reference when used with dual supplies only. The circuit of Figure 13 could prove useful in such applications. It provides a V_{SS} of −5V, the +5V reference and V_{DD} of +11.4V to +16.5V from a single +16.4V to +21.5V power supply rail (in battery applications two 9V batteries in series). The AD584 is a pin-programmable precision voltage reference. The AD380 op-amp buffer establishes the "ground" for the AD7226 midway between 0 and +10V. Hence, pin 1 of the AD584 can be used as the +5V reference for the AD7226. The V− of the input signal is used to provide a V_{SS} of −5V. If the input voltage can exceed the limits above (i.e., +16.4V to +21.5V) a zener diode may be required to provide a regulated supply voltage to the V_{DD} pin of the AD7226. The voltage at the V_{DD} pin must never exceed +17V with respect to the AD7226 "ground".

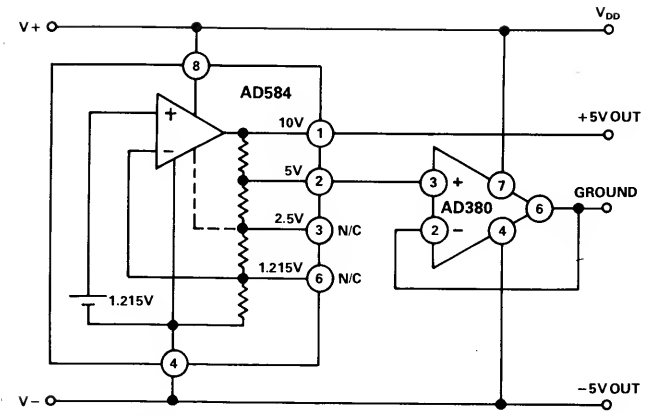

Figure 13. Voltage Splitting Using AD584

5V SINGLE SUPPLY OPERATION

The AD7226 can be operated from a single +5V power supply rail, but because the output amplifier now loses a considerable amount of headroom, the performance of the part is degraded. However, one important parameter which retains its specified performance is differential nonlinearity. At a single +5V supply this remains within ±1LSB which ensures that the AD7226 will remain monotonic over the output voltage range.

This monotonic operation makes the AD7226, at single +5V supply, suitable for applications where the absolute value (or accuracy) of the output voltage is not important but where it is essential that the output increases as the digital code increases. An example of this type of application has already been outlined in this application note: trimming the offset of operational amplifiers.

The required overhead voltage of 4V between the reference voltage and the V_{DD} input must still be maintained under these conditions. This means that the reference voltages must remain below 1V to ensure monotonic operation. At these low reference voltages, the output offset voltage is obviously very large with respect to the input reference and the relative accuracy is also degraded. However, the output voltage does increase as the input digital code varies from 0 to 255. This can be seen from the plot of Figure 14 which shows differential nonlinearity for single +5V supply at a reference of 600mV. Figure 15 shows a plot of relative accuracy for the same part under the same conditions. Additionally, the digital input threshold levels and digital input currents are not affected by operating the AD7226 from the single +5V supply rail.

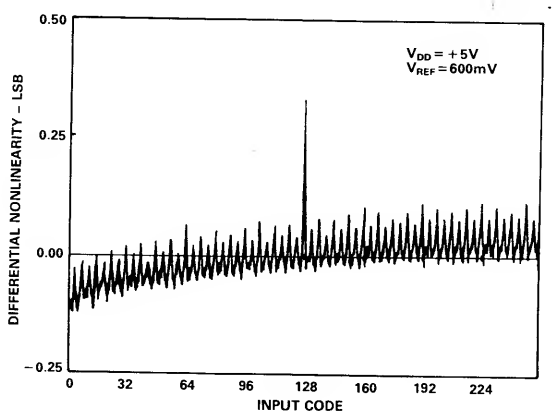

Figure 14. Differential Nonlinearity at 5V V_{DD}

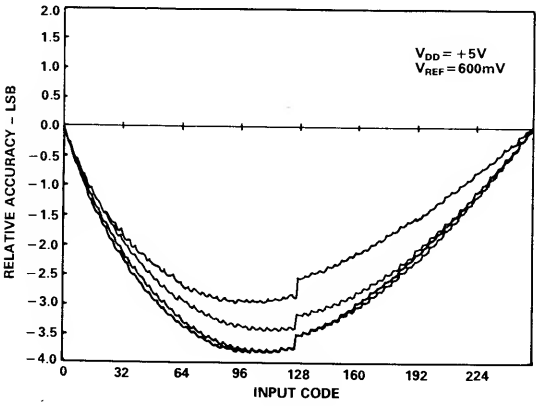

Figure 15. Relative Accuracy at 5V V_{DD}